COMPENSATION CIRCUIT AND METHOD TO COMPENSATE NONLINEAR DISTORTIONS OF AN A/D CONVERTER

BACKGROUND OF THE INVENTION

The invention relates to the field of analog-to-digital signal conversion, and in particular to a compensation circuit to compensate nonlinear distortions of an analog-to-digital (A/D) converter.

A/D converters are a critical component in integrated circuits having mixed signal processing (i.e., analog and digital signal processing). Requirements related to the linearity of the A/D converter are quite difficult to achieve given the usual tolerances for analog components. The measures required for this purpose in the area of analog design entail high cost and/or high current consumption by the circuit.

In order to prevent nonlinear distortions in the analog-to-digital conversion process of the A/D converter, compensation circuits are employed to compensate for these nonlinear distortions of the A/D converter. The compensation circuits have an analog signal input, and are typically located on the input side of the A/D converter.

There is a need for a compensation circuit that compensates for nonlinear distortions of an A/D converter, and requires a simplified overall analog design together with, preferably, reduced current consumption.

SUMMARY OF THE INVENTION

A compensation circuit to compensate nonlinear distortions of an A/D converter may include a signal input and a compensation circuit composed of digital circuit elements to digitally compensate nonlinear distortions, the signal input as the compensation input being a digital signal input to supply a signal outputted in distorted form by the A/D converter. Implementation is thus in

the form of an output-side digital compensation or distortion correction of the nonlinear distortions from an input-side A/D converter. The digital circuit elements required for this purpose are inexpensive and readily available based on a simple digital circuit design. Advantageously, it is no longer necessary to incur high costs or have increased current consumption based on a compensation circuit added on the input-side of, or integrated into, the A/D converter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustration of a compensation circuit to compensate for nonlinear distortions of an A/D converter;

FIG. 2 is a block diagram illustration of a circuit to determine a test signal;

FIG. 3 is a block diagram illustration of a circuit for the iterative calculation of correction coefficients; and

FIG. 4 is a block diagram illustration of an alternative circuit for the iterative calculation of correction coefficients using a look-up table.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a block diagram illustration of a compensation circuit to compensate for nonlinear distortions of an A/D converter. The compensation circuit in the example is composed of an analog section, shown at left, and a digital section shown on the right. An analog input signal x(t) is supplied to an A/D converter ADC 1, which provides a digital sequence x_n corresponding to the analog input signal x(t). When a conventional A/D converter 1 is used, the digital sequence x_n from this converter exhibits nonlinear distortion. The index n represents the sequence of sampling values x_n, n = 0, 1, 2, ...

The A/D-converted sequence x_n is input of a compensation circuit 2, which compensates or corrects the nonlinear distortion created by the A/D converter 1. The compensation circuit 2 provides compensated digital data y_n.

The compensation circuit 2 receives coefficients $c_1, c_2, \ldots c_K, c_0$ that have been determined or calculated based on the nonlinear distortion response of the A/D converter 1. The index $k = 1, 2, \ldots, K$ here functions as the consecutive index for the coefficients c_k of compensation.

The circuit of this design includes an A/D converter 1 together with the compensation circuit 2 to which a set of coefficients $c_1, \ldots c_K$ is supplied offers a simple design which enables an analog-to-digital conversion of an analog signal x(t) to form a sequence of compensated digital data y_n which does not suffer from nonlinear distortion.

A coefficient computation unit 100 determines the coefficients $c_1, \ldots c_K$. These additional components are advantageously active only during a configuration phase. As an alternative to the circuit described below, it is also possible to employ a memory in which a set of coefficients $c_1, \ldots c_K$, determined previously only once, is stored which may be applied generally for the compensation. However, the preferred approach is the circuit design described below which provides an adjustment of the coefficients $c_1, \ldots c_K$ to the actual and/or instantaneous conditions.

Referring to FIG. 1, a test signal s(t) is generated by a test signal generator 3 and applied during the configuration phase to the input of the A/D converter 1. The test signal generator 3 also provides either the parameters s_n to generate the analog test signal s(t) or a sequence of digital test signal data S_n corresponding to this analog test signal s(t). These parameters s_n or test signal data S_n are fed to a coefficient determination system 5 and/or to a test signal check device 4.

The coefficient determination system 5 determines the coefficients $c_1, \ldots c_K$ to be used by the compensation circuit 2. The coefficient determination system 5 receives the digital data x_n from the

A/D converter 1. The coefficient determination system 5 also receives distortion data or difference data D_n on a line 102. The difference data D_n are provided by a subtracter 6 to which the sequence of the compensated digital data y_n is fed from the output of the compensation circuit 2. The subtracter 6 also receives a sequence of digital signal data S_n either directly or indirectly through the test signal check device 4. The sequence of digital signal data S_n corresponds in the configuration phase to a signal map of the test signal, whereby, after appropriate determination of coefficients has been effected, this signal map is as undistorted as possible, or ideally is completely undistorted.

During the configuration phase, the analog test signal s(t) is generated and fed to the A/D converter 1, which provides the sequence of digital data x_n to the compensation circuit 2 and the coefficient determination circuit 5. If the set of coefficients c_1, ... c_K is not available, the compensation circuit 2 outputs the sequence of digital data x_n as the sequence of compensated digital data y_n (i.e., $y_n = x_n$). This data is fed to the subtracter 6, which is also supplied with a corresponding sequence of digital test signal data S_n matching an undistorted data set. After subtraction of the two sequences of data (y_n - S_n), the data sequence of the difference signal D_n on a line 102 is supplied to the coefficient determination system 5. According to a preferred embodiment, a test signal s(t) is subsequently sent by the test signal generator 3, which may also be composed of a memory with an analog test signal s(t) and a corresponding digital parameter set s_n, to the A/D converter 1. The sequence of digital data x_n generated by the A/D converter 1 is subsequently compensated by the compensation circuit 2 in accordance with this supplied set of coefficients c_1, ... c_K, such that the sequence of compensated digital data y_n is output, ideally with already optimized coefficients c_1, ... c_K, without nonlinear distortion. The sequence of compensated digital data y_n is in turn fed to the subtracter 6 in which, after subtraction using the corresponding values of the sequence of digital test signal data S_n, the sequence of data D_n of the difference signal is again generated. This difference

data D_n is again fed to the coefficient determination system 5 which, in the event difference data D_n does not equal zero or exceeds predetermined threshold values, implements another, or preferably, an iteratively improved determination of coefficients to provide improved coefficients $c_1, \ldots c_K$.

After a sufficiently distortion-corrected or compensated set of coefficients $c_1, \ldots c_K$ has been determined, the configuration phase ends, after which the circuit composed of the A/D converter 1 and the compensation circuit 2 implements a conversion and compensation of the analog signal x(t) to form a sequence of compensated digital data y_n.

A configuration phase is initiated at regular intervals to check the set of coefficients used, $c_1, \ldots c_K$ in terms of their current validity. In this way drifting nonlinear distortions caused for example by the circuit heating up or other interfering effects from the environment can be compensated.

The configuration phase is turned on and off as needed so that any slow changes in nonlinear distortions can be detected early enough and then compensated. It is, of course, in principle also possible to implement a predetermination and consideration of anticipated additional degradations or improvements related to the generation of distortions.

A control device 104 is advantageously employed to control the compensation circuit, the control device 104 being connected to a time-monitoring device, specifically, a timer 106. In addition to turning the configuration phase on and off, the control device 104 also controls the individual components through, for example, a bus 7.

In particular, it is possible to provide different types of test signals s(t), s_n for different application areas of the circuit so that coefficients $c_1, \ldots c_K$ may, for example, be optimally adjusted for a low-frequency or high-frequency analog signal x(t).

The following discussion examines in more detail the circuit components and the operational sequences of the method with reference to the mathematical background.

The configuration phase starts with an analog test signal s(t),

to which the theoretical uncorrupted sampling values

$$S_n = s\left(\frac{n}{Fs}\right),$$

correspond after analog-to-digital conversion, without nonlinear distortion, which values are in turn to be output after optimal compensation from the compensation circuit 2 as the sequence of compensated digital data y_n. Here n is a consecutive index of the set of natural numbers, while F_s is the sampling frequency of the A/D converter 1.

After analog-to-digital conversion has been performed on the analog test signal s(t) the sequence of digital data x_n is supplied to its output based according to the expression

$$x_n = s_n + d_n.$$

The sequence of digital data x_n thus corresponds to the summation of correct theoretical and uncorrupted sampling values s_n, and the respective distortion data value d_n which matches the corresponding distortion by the A/D converter 1.

The digital compensation circuit 2 which uses the coefficients c_1, ... c_K to generate the sequence of compensated digital signals y_n that are ultimately to be output must therefore perform a compensation having the characteristic that may be described by a K^{th}-order polynomial:

$$(1) \qquad y_n = \sum_{k=l}^{K} c_k \cdot x_n^k = v \cdot s_n + D_n = S_n + D_n .$$

Here the coefficient values c_k with $k = 1, 2, \ldots K$ are adaptive coefficients, that is, coefficients which may be adjusted as necessary. The output signal, or sequence of outputted compensated digital data y_n contains a map of the test signal or of the sequence of digital test signal data S_n plus a possible change v, specifically, amplification or ~~distortion~~ attenuation. The sequence of compensated digital data S_n is thus the product of a distortion factor v and the sequence of digital test signal data s_n which may be described by

$$S_n = v \cdot s_n ,$$

where the effective distortions of the switching sequence of the A/D converter 1 and, in the event of insufficient compensation, of the compensation circuit 2 may be described by the sequence of difference data D_n according to the expression

$$(2) \qquad D_n = y_n - S_n.$$

Since the parameters s_n of the test signal are known, the sequence of output signal data S_n may be extracted from the sequence of compensated digital data y_n by the test signal check device 4 to enable the actual distortion data or difference data D_n in data y_n to be calculated at the output of the compensation circuit 2. In addition, the gradients of the rms distortion may be calculated using the expression

$$\frac{\partial D_n{}^2}{\partial c_k} = 2 \cdot (y_n - S_n) \cdot x_n^k = 2 \cdot D_n \cdot x_n^k .$$

The use of an iterative method allows the set of coefficients c_k to converge. To this end, the formulation

$$(3) \qquad c_k^{n+1} = c_k{}^n - G \cdot D_n \cdot x_n^k$$

may be selected so as ultimately to minimize the rms distortion or output. A parameter G is introduced in equation (3) as a stability criterion, which parameter at the same time provides for the highest possible convergence rate. The term c_k^n describes the value of the coefficients c_k in the n^{th} iteration step, the coefficient of compensation c_k again having the consecutive index $k = 1, ..., K$. The iteration steps are preferably counted from the value zero, so that $n = 0, 1,...$.

In an especially preferred embodiment, a sinusoidal test signal $s(t) = \sin[2\pi t]$ is preferably used as the test signal to perform the nonlinear compensation since it is then simpler for the A/D converter 1 to determine the structure of the distortions, and is possibly simpler for the compensation circuit 2 to determine additional distortions. A nonlinearly distorting A/D converter 1 having a sinusoidal input signal at a frequency F_t produces harmonics on frequencies $p \cdot F_t$, which may be folded back by sampling to form

$$f_k = \begin{cases} (p \cdot F_t)_{\bmod Fs} & (p \cdot F_t)_{\bmod Fs} \le \dfrac{F_s}{2} \\ F_s - (p \cdot F_t)_{\bmod Fs} & (p \cdot F_t)_{\bmod Fs} \ge \dfrac{F_s}{2} \end{cases}.$$

Here p = 2, 3, ..., M is the consecutive index of the frequency calculation.

If the first harmonics are significant, specifically, if p = 2, ..., M applies, the test frequency F_t should be selected such that the frequency band 2B is maximized around the fundamental where none of the first M harmonics fold back according to the expression

$$\text{(4)} \qquad B = \max_{F_t} \left\{ \min_{p=2,\ldots,M} \{|F_t - fp|\} \right\}.$$

The extraction of the test signal or sequence of output signal data S_n may be implemented using a known method of carrier processing. Another factor which must be taken into account is that the test signal s(t) or the sequence of output signal data S_n assigned to this signal are amplitude-conforming.

To this end, a circuit may be used that is based on an I/Q demodulator (I: in-phase, Q: quadrature phase) and a Cordic circuit 43, and calculates the phase and amplitude of the input sequence of digital data y_n. FIG. 2 provides an example of this circuit.

Frequency, amplitude and direct current (DC) are recovered by feedback using the method known from automatic control engineering. A proportional and integral (PI) control is employed to determine the frequency. To determine amplitude and direct current, a ∓PI-control is used in which

only the proportional components are employed. The control parameters used are the P-component of the amplitude control C_a, the P-component for the DC components C_{dc}, and the P-component and I-component of the frequency control C_p or C_i, which components are intended at the same time to meet the stability criterion for a control loop and to ensure the fastest possible transient.

The supplied sequence of digital data y_n is input to multipliers 41a, 41b. A sinusoidal signal sin[2πt] as the signal sequence to be multiplied is fed to the first of the multipliers 41a by a sinusoidal tone generator 41. Analogously, a cosine signal sequence cos[2πt] is supplied by the sinusoidal tone generator to the second multiplier 41b. After multiplication, the two data sequences are each fed to an associated filter 42a, 42b, respectively, with undersampling P. After filtering, the I-separated and Q-separated signal components are supplied to a Cordic circuit 43 which determines, a corresponding amplitude and corresponding phase that are supplied through two outputs.

The sequence representing the amplitude is input to a subtractor 44a, which also receives a feedback signal on a line 202. The subtractor 44a provides a difference signal to multiplier 44b, which multiplies the difference signal by a coefficient value C_a , and the resultant product is output to a summer 44c. The summer 44c sums the product with the past value. The summer 44c provides a signal sequence to a delay element 44d, which provides a signal sequence to a delay element 44d, which provides an output signal to a multiplier 44e. The multiplier 44e also receives a cosine signal cos[2πt] and provides the resultant product on a line 204. This system is ultimately used to determine the sequence of output signal data S_n that is then supplied to the difference-forming subtracter 6, which in turn has the sequence of digital data y_n applied to it through the second input.

The Cordic circuit 43 also outputs a corresponding phase or sequence of phase data on a line 206. This data is also fed to a circuit composed of a plurality of components 45. In the embodiment shown, this circuit is composed of two parallel multipliers 45b, 45a to which additionally a

coefficient value C_p or a coefficient value C_i is supplied. The output signal of the multiplier 45a is fed to an adder 45c, the output signal of which is supplied both to an inverter (z^{-1}) 45d and to a second adder 45e. The output signal of the inverter 45d is fed to the second input of the adder 45c. Through another input, the second adder 45e receives data from the multiplier 45b in which coefficient value C_p is up-multiplied for the phase data. The output data from this adder 45e are fed to another adder 45f which has two additional inputs. A frequency ratio F_t/F_s including the test frequency F_t of the A/D converter 1 and the sampling frequency is supplied through the first additional input. An output value of the inverter (z^{-1}) 45g connected after the adder 45f is fed through the second input. Output values of this inverter 45g are supplied as the timing variable t to an input of the sinusoidal tone generator 41.

In addition, a DC component DC_n is filtered out and extracted from the sequence of digital compensated data y_n outputted from the compensation circuit 2. To this end, the digital compensated data y_n are supplied to a circuit 46 composed of a subtracter 46a, a multiplier 46b, a adder 46c, and an inverter (z^{-1}) 46d. A control parameter C_{dc} is applied through the second input to the multiplier 46b. Control parameter C_{dc} determines the rate of the transient. The output data sequence from the inverter 46d is supplied to the inputs of the subtracter 46a and the adder 46c, as well as to the subtracter 6 generating the difference data D_n.

Referring to FIG. 2, the frequency F_t is thus derived using a phase-locked loop (PLL). The input signal corresponding to the sequence of compensated digital data y_n is split into I-component and Q-component that are then filtered by the low-pass filter 426 of critical frequency B and undersampled. From the filtered I-component and Q-component, the Cordic circuit 43 then computes the amplitude and phase between input signal y_n and the locally generated sinusoidal tone from the sinusoidal tone generator 41. The phase is passed to the PI control as the error signal. After

a settling time, the sinusoidal tone generator 41 generates in its cosine branch a signal synchronized with the test tone. The coefficients C_p and C_i, and test frequency F_t as the known parameters determine the PI control. The amplitude is derived iteratively from the amplitude output of the Cordic circuit 43 using the control parameter C_a. The DC components are filtered and extracted from the output signal using control parameter C_{dc}. The complete circuit composed of the test signal check device 4 (FIG. 1) and following the subtracter 6 (FIG. 1) finally generates a sequence of difference data D_n according to equation (3) proportional to the nonlinear distortions.

Advantageously, available carrier-processing systems and carrier-processing methods may be utilized for the purpose of implementing this circuit. What must be added are the circuits for the amplitude and DC components.

An especially preferred embodiment of compensation circuit 2 is constructed segment-by-segment, as shown in FIG. 3.

The data sequence x_n outputted by the A/D converter 1 is input to the compensation circuit 2 to a parallel system of multipliers 21. At the same time, the same input signal, i.e., once again the corresponding data value of data sequence x_n, is fed to the second input of first multiplier 21_2 so that a squaring is effected. The output of this first multiplier 21_2 is supplied to the input of the second multiplier 21_3, and so on, such that at each subsequent stage the exponent is increased by the value one up to a value x_n^K.

As a result, an exponentiation is effected, where each exponentiation step has an output so that values for digital data with exponentiations x_n^1, x_n^2, ..., x_n^K are output from the input and the field of the multipliers 21. These are then fed to another field of multipliers 22, whereby a multiplication is performed with one each of the corresponding coefficients $\cancel{e_k(m)}c_k(m)$ where k = 1, 2, ..., K. What is described is thus a multi-element system with the coefficients $c_k(m)$of the

compensation in the m^{th} segment with $m = 0, 1, 2, ..., N-1$ as the m^{th} segment of the amplitude range. Accordingly, the nonexponentiated value or nonexponentiated data sequence x_n^1 as well as the coefficient $c_1(m)$ are entered in the first multiplier 22_1 of the second multiplication field 22. The once exponentiated data value x_n^2 and the second coefficient $c_2(m)$ are entered in the second multiplier 22_2, etc. The output values of the multipliers $22_1, 22_2, ..., 22_K$ of second multiplication field 22 are fed to an adder 23 which performs an addition of all input values, and also of the zeroth coefficient $c_0(m)$, then outputs the sequence of compensated digital data y_n.

The sequence of digital data x_n output by the A/D converter 1 is also fed to the coefficient determination system 5, where a rounding operation is performed in an index determination device 51, taking into account the N segments during the determination of the index m. Here the sequence of digital data x_n with its respective value increased by one is divided by two, then multiplied by the number of segments N. The thus generated segment index m on a line 302 is fed to a coefficient memory system 52 that is composed of a plurality of m parallel memory components $52_0, 52_1, ..., 52_{N-1}$. The respective coefficients $c_1(m), c_2(m), ..., c_K(m)$ und $c_0(m)$ are stored in the individual segments of this coefficient memory system 52. For each stored index m, there is an output to an adder $53_1, 53_2, ..., 53_K, 53_0$, the output of which in turn is fed back to the same segment of coefficient memory system 52. The result from a multiplier $54_1, 54_2, ..., 54_K$ is entered in the second input of the adders $53_1, ...$. Each correspondingly exponentiated value of the sequence of digital data $x_n^1, x_n^2, ..., x_n^K$ is fed to the inputs of the multipliers $54_1, 54_2, ..., 54_K$. Supplied to each second input of the multipliers $54_1, 54_2, ..., 54_K$ is the result of a multiplier 55 to which both the corresponding values for difference data D_n and the negative parameter -G serving as the stability criterion are supplied. Only the value for the difference data D_n, multiplied by the negative parameter -G, is supplied to the adder 53_0 at the adder's second input.

Using a circuit of this type, the compensation circuit 2 may be implemented on a segment-by-segment basis. The range of input data values, that is , the sequence of digital data x_n, from the A/D converter 1 with data values from -1 to +1 is, uniformly distributed among N segments according to the expression

$$-1+\frac{2}{N}m \leq x_n \leq -1+\frac{2}{N}(m+1),$$

where the segment index m lies between 0 and N-1. As a result, one coefficient set $\{c_0(m), c_1(m), ..., c_K(m)\}$ is assigned to each segment. Based on segmental interpolation of the characteristic, zeroth coefficients $c_0(m)$ are added in, so that for the sequence of compensated digital data y_n outputted from the compensation circuit 2 the following expression applies:

$$(5) \qquad y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k \text{ where } m = \left\lfloor N \cdot \frac{x_n+1}{2} \right\rfloor,$$

where $\lfloor\ \rfloor$ represents the rounding operation.

The equation (5) for compensation in the compensation circuit 2, and the iterative calculation of coefficients according to equation (3) may be effectively implemented together, as FIG. 3 illustrates. In a memory of size N x (K+1), here the coefficient memory system 52, N sets of K+1 coefficients each $c_1(m)$, $c_2(m)$, ..., $c_K(m)$, and $c_0(m)$ are stored for the respective m = 0, 1, 2, ..., N-1. For each sampling instant, the index m is derived according to equation (5) from the input signal, i.e., from the applied value for the sequence of digital data x_n, and assigned to the corresponding

coefficient set $52_0, 52_1, \ldots, 52_{N-1}$, then applied accordingly within the compensation circuit 2. Also in this procedure, the stored value for each coefficient is iteratively improved according to equation (3) and stored in the same memory location.

As shown in FIG. 4, in a certain case the method with segmental interpolation may be simplified with $N = 2^B$. For this purpose, it is necessary that the number N of segments agree with the resolution of the signal or the sequence of digital data x_n, i.e., $N = 2^B$ applies, where B is the number of bits per sampling value given a signal range between -2^{B-1} and $2^{B-1}-1$ and only one coefficient per segment, i.e., K = 0.

The circuit of FIG. 3 is thereby reduced to the circuit of FIG. 4 which has, following the index determination device 51 for determining the index m, a look-up table with 2^B adaptive coefficients $c_0(m)$in memory fields $52_0, \ldots, 52_{N-1}$. In this arrangement, all the multipliers 54 are eliminated so that only the first addition stage with adders 53_1, ... remains, as described above.

Initial synthetic calculations using a sinusoidal tone as the test signal s(t) and a mathematical model of the analog-to-digital characteristic with frequencies $F_s = 40.5$ MHz, $F_t = 1.84$ MHz, the A/D model with coefficients for the calculation based on $0.9895x + 0.0028x^2 + 0.024x^3 - 0.0064x^4$ and for compensation N = 1 segments, and a maximum running index of m with K = 4, produced significant improvements. After analog-to-digital conversion, the initial value was -60.3 dB, and after compensation the value was 80.9 dB – yielding a significant improvement of 20.5 dB. In the case of one measurement (K3), the improvement found was -47.2 dB after A/D conversion, as compared with -56.3 dB after compensation, giving an improvement of 9.1 dB. The ratio of distortions to outputs after A/D conversion was -46.8 dB, as compared with -55.3 dB after compensation – producing an improvement of 8.4 dB.

In place of a plurality of individual components, as described above, an implementation is also possible in an analogously capable computer chip, or in a monolithically fabricated semiconductor device in the form of an integrated circuit or the like.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: